RF MEMS Switch Packaging

IMAPS New England 44th Symposium & Expo, Boxboro, MA

Session: RF and Microwave - Innovations and Emerging Technologies

May 3, 2017

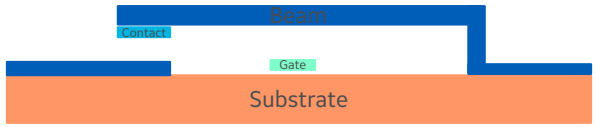
Agenda

- Introduction
- Packaging challenges
- Solutions
- Test Results
- Future Work
- Summary

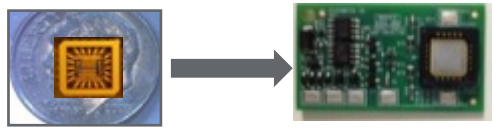
What is GE Digital-Micro-Switch Technology?

A novel micro-mechanical ***switch*** architecture based on an ultra-reliable material set, incorporating new design and processing techniques

Ohmic contact switch with cantilever beam and electrostatic actuation



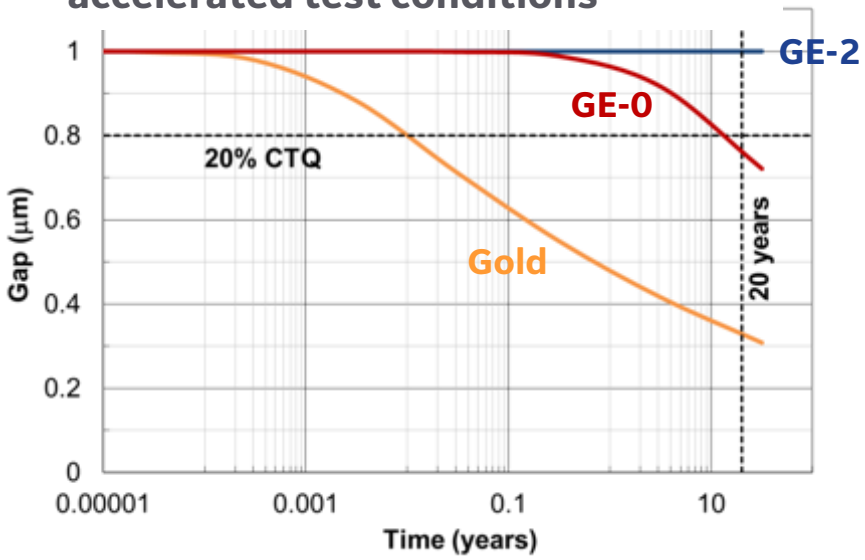
Smart RF and Power relay systems
High-power, High-reliability



240V/10A
AC/DC Relay

400V/2A
RF Relay

Beam lifetime comparison under accelerated test conditions



Over 10+ years of development, over 40 patent families and know-how covering materials & fabrication processes, as well as system architecture, design, test

GE DMS technology can enable new, disruptive products: High-power, High-reliability SMART RELAY SYSTEMS

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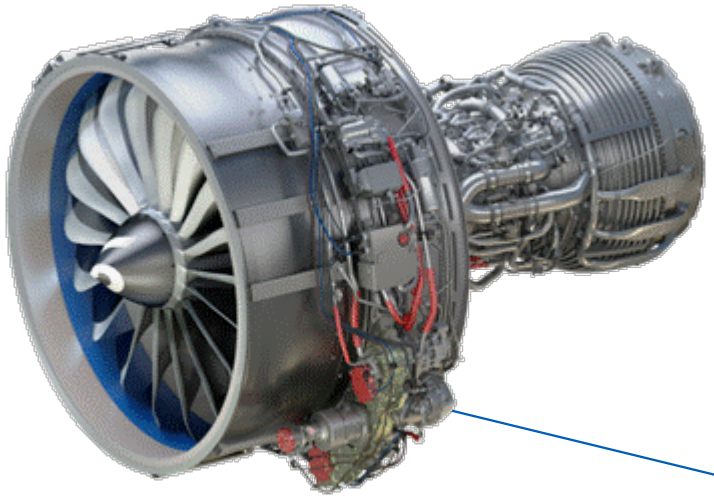
The GE Approach

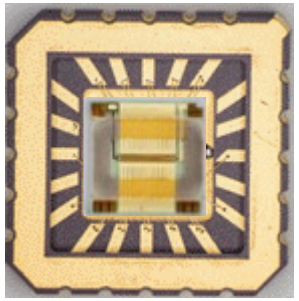
imagination at work

- GE approached MEMS reliability issues not as a semiconductor company, but with decades of experience in high-performance alloys

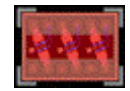


- GE's breakthrough innovations in materials and processing enable true Product Development Platform:

- High-Reliability: Shipping in production to a 3B cycles spec
- High-power capable: Opens up new markets, larger TAM
- Simple design, <12 mask layers: Can scale with volume to very low cost
- Simple design, wide design space: Shorter design cycles = more products



9mm x 9mm



1mm x 1.5mm

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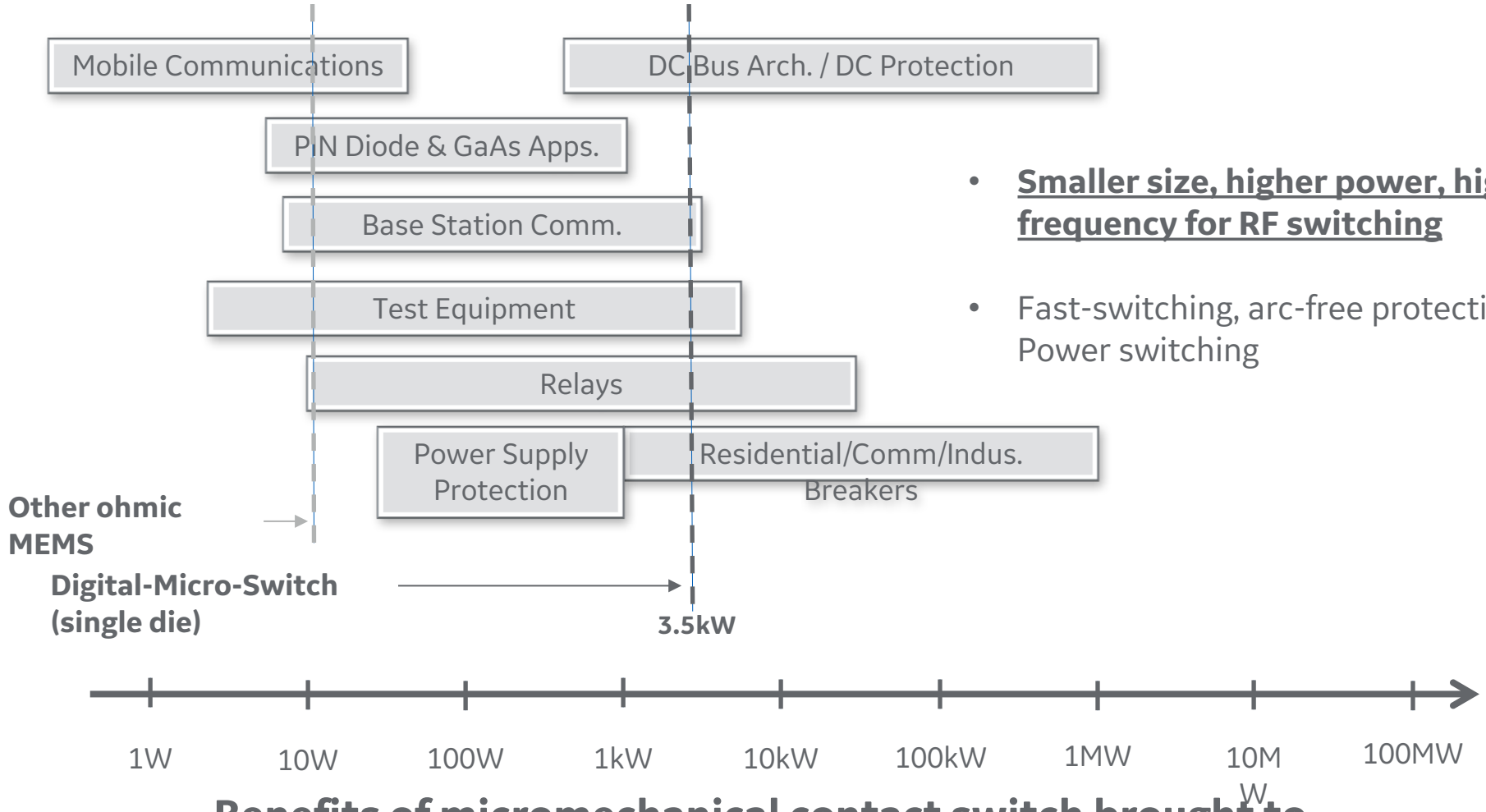
Digital-Micro-Switch Applications

Step function improvements in power handling and reliability



- **<u>Smaller size, higher power, higher frequency for RF switching</u>**
- Fast-switching, arc-free protection for Power switching

Benefits of micromechanical contact switch brought to many more applications

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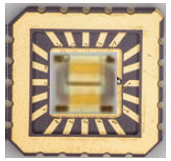
MEMS Product Portfolio - 2017

HV Switch Products

MM7100



- 9mm x 9mm LCC
- WL bonded
- **500V/1A <128MHz**

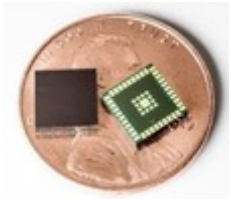
MM7110

- 6mm x 14mm SIP
- **1000V/1A <128MHz**
- Integrated driver, passives

- Target Markets: MRI, general purpose HV switch

RF Tuning Products

MM3100

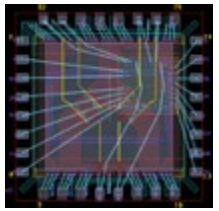


- 6mm x 6mm LGA / BGA
- 6 channels, 25W/channel
- DC to 3GHz
- Embedded controller

- Target Markets: A/D, Industrial
- Target Applications: Tunable UHF/VHF/HF radios, general purpose EM relay replacement, WPT

RF Switching Products

MM5120

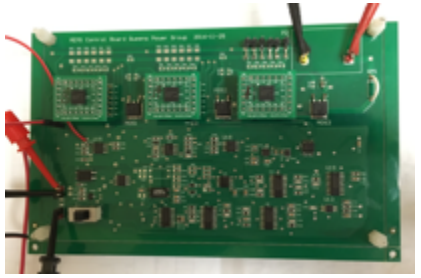


- 5mm x 5mm QFN
- SPDT, 25W/channel
- DC-12GHz
- Embedded controller with Vboost
- Bare-die option to 18GHz+

- Target Market: A/D, Test & Measurement, Wireless Infra.
- Target Applications: Switched filters, switch matrix, high power RF switching, EM replacement

Power Relay Products

Smart Power Relay Prototype



- 6” x 4” proto board
- 200V/10A DC power relay
- Integrated current sense
- No heat sink

- Target Market: Industrial, Test & Measurement

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RF Packaging Considerations

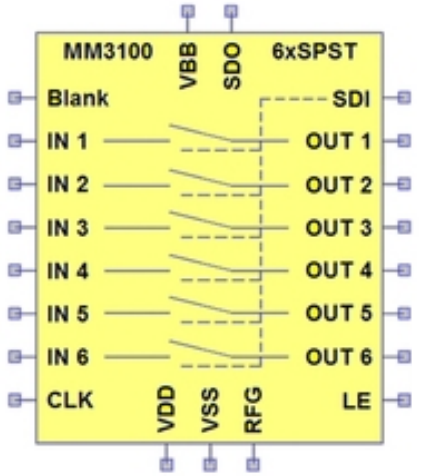
Package Design Considerations
- Maintain device hermeticity
- Compatible materials: Die attach films, mold compound, substrate
- Package geometry
- System-in-package component interaction

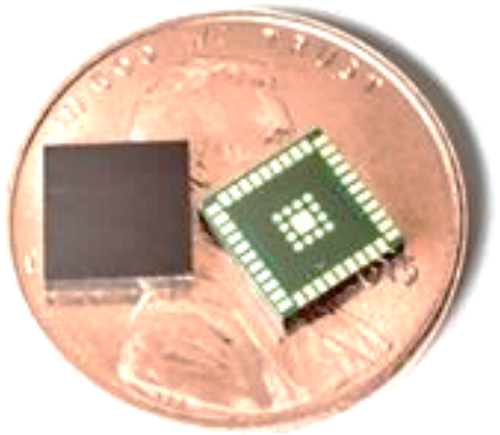
Package Design Approach
- Device-package co-design
- Design iteration
- Design for test
- Experimental validation

RF Package Design Case Study

MM3100 – 6 Channel SPST Digital Micro-switch

- **Hermetic 6mm x 6mm x 1.3mm LGA Package**
- **Integrated SPI Bus Gate Control**
- DC to >3 GHz Frequency Range
- 25 Watt (CW), 200W (Pulsed) Max Power Handling
- Low On-State Insertion Loss < 0.3 dB @ 3 GHz
- Low On-State Resistance < 0.75 Ω
- -25dB Isolation @ 3 GHz
- Maximum voltage (AC or DC): +200 Volt on RF Input
- < 10us On/Off Switching Time
- High Reliability > 3 Billion Switching Operations





6mm QFN/BGA

- Target Markets: A/D, Industrial
- Target Applications: Tunable UHF/VHF/HF radios, general purpose EM relay replacement, WPT

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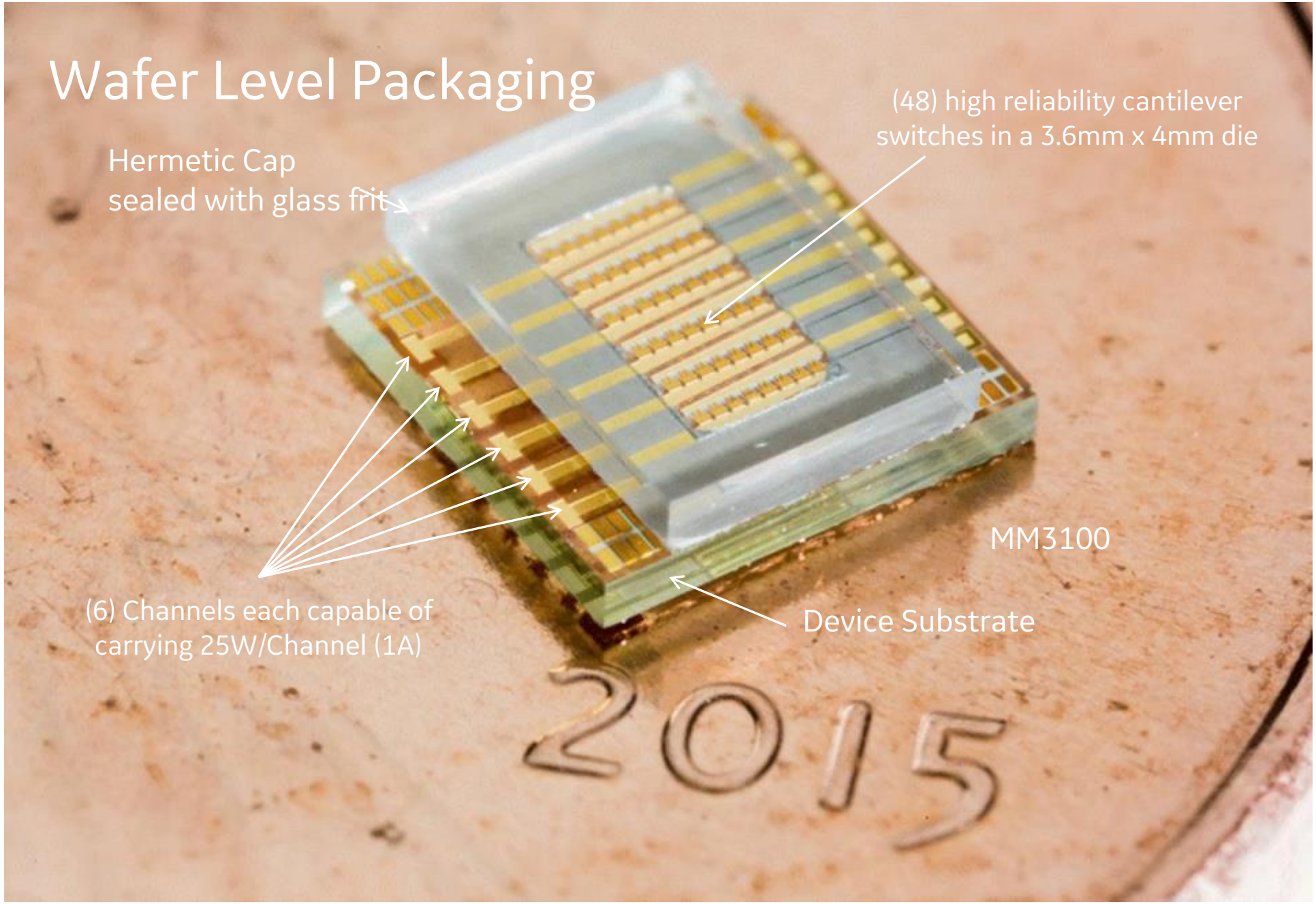
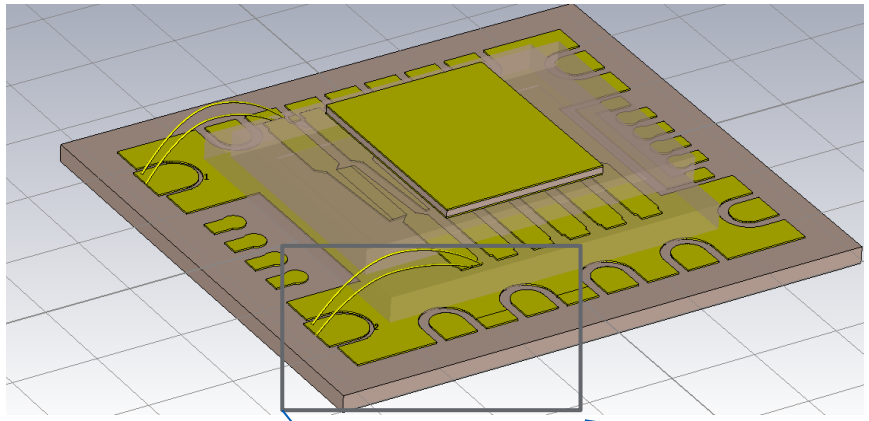
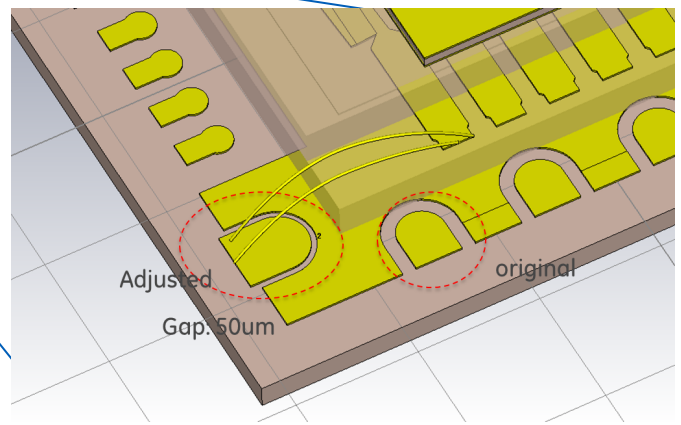
Wafer Level Packaging

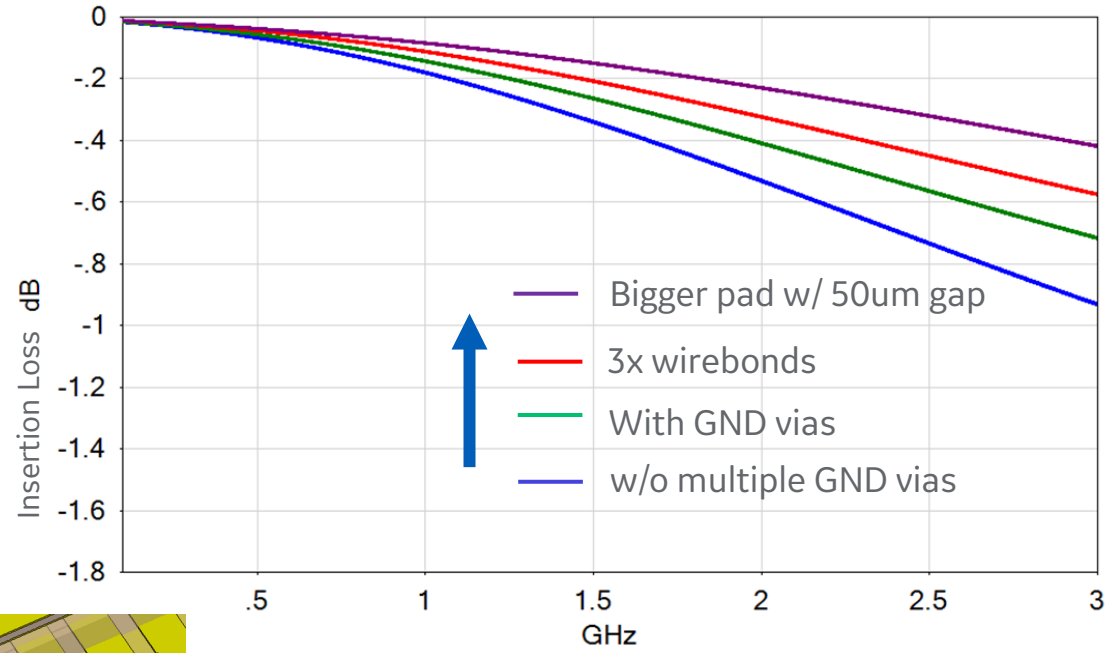


Substrate Design Considerations

RF Simulation







Design changes improved performance

Primary drivers

- Grounding
- Thickness
- Assembly constraints
  - ✓ Pad size for wire-bonding
  - ✓ Wire-bond keep out distance

- Substrate material – FR4 (DK=4.3, tanδ=0.02)
- Thickness: 180 µm
- 2 metal layers

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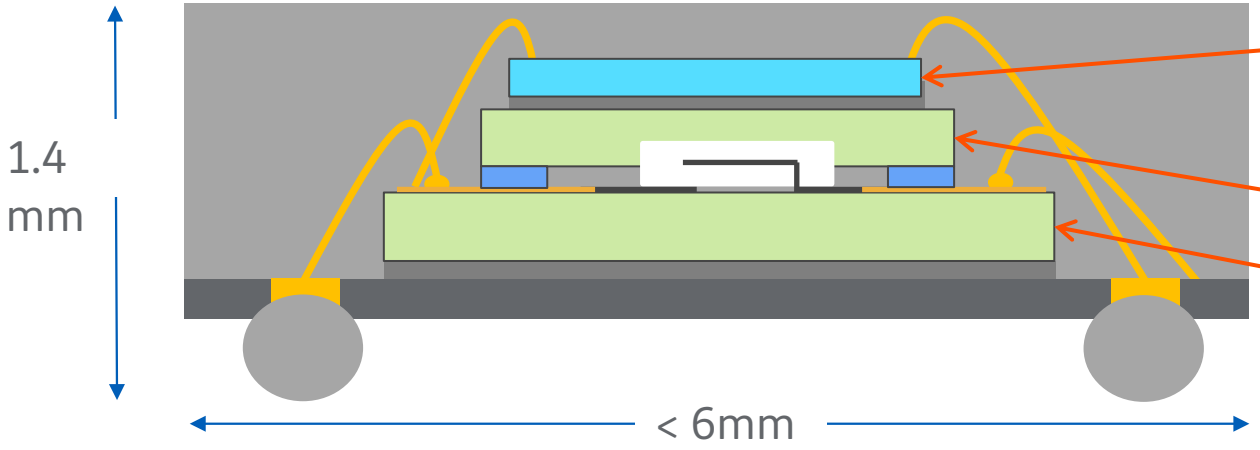
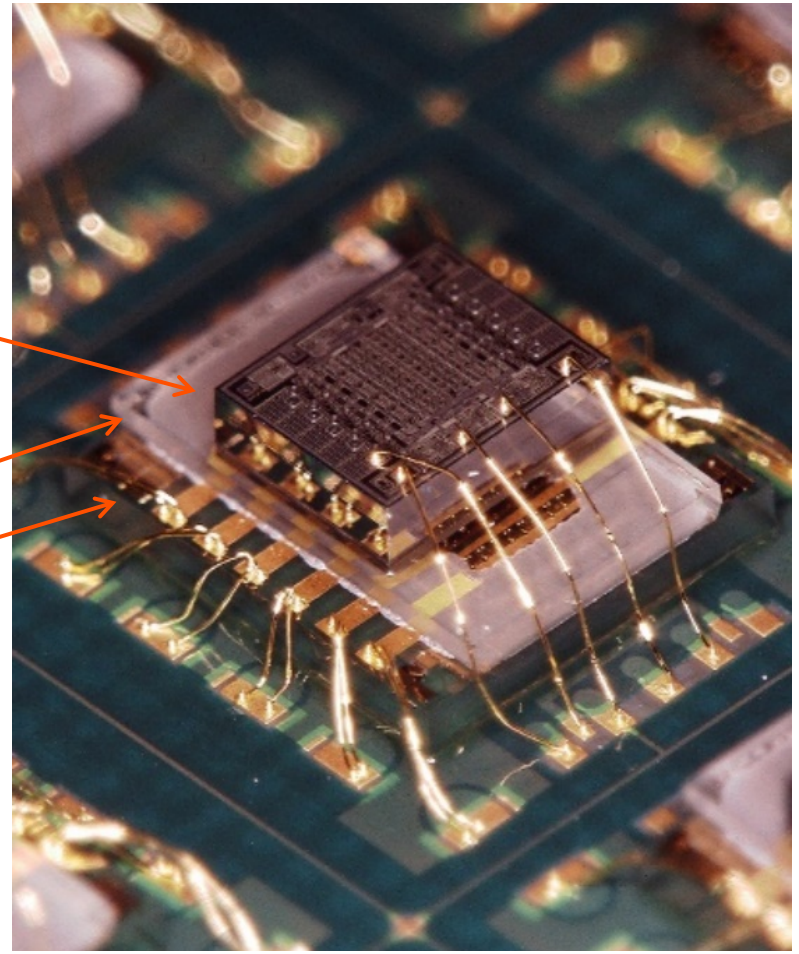
Stacked Die Considerations

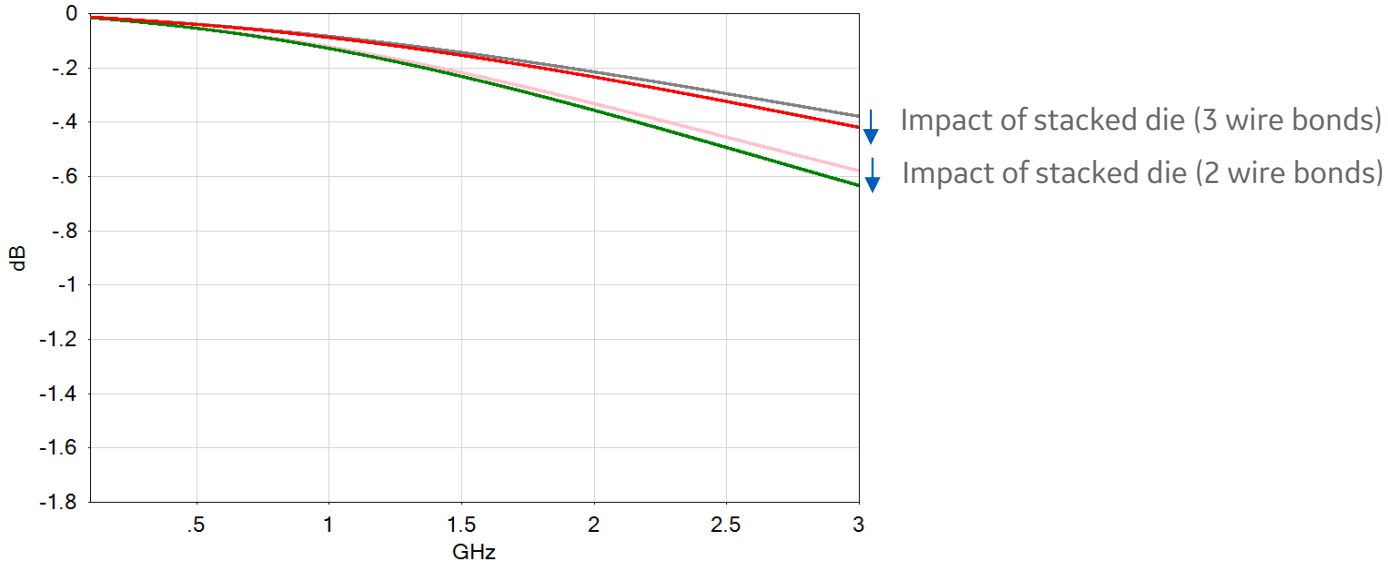




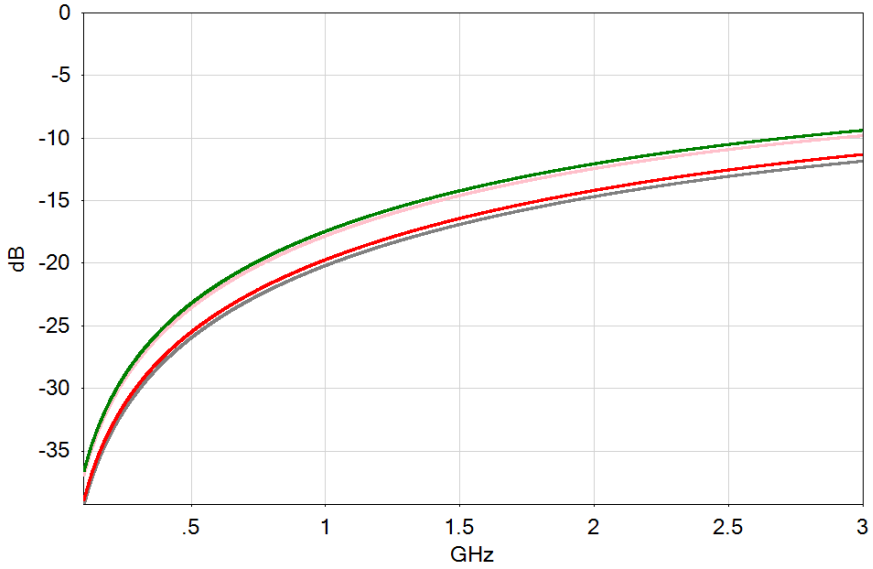
- RF Implications – Isolation loss
- Wire sweep
- Keep out regions

Stacked Die Impact

Simulation Results



Insertion loss



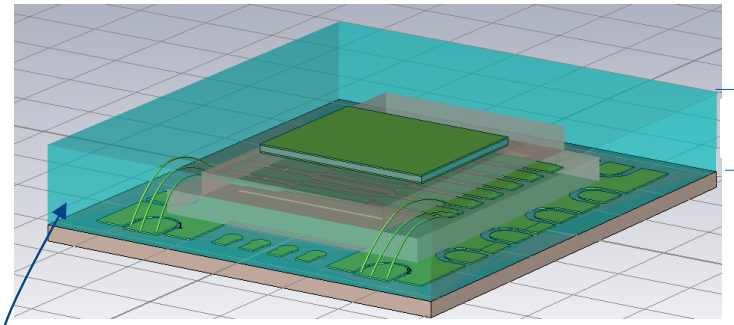
Return loss

Minimized Impact of die stacking with appropriate selection of:

- Die attach film
- Cap thickness
- Die thickness and placement location

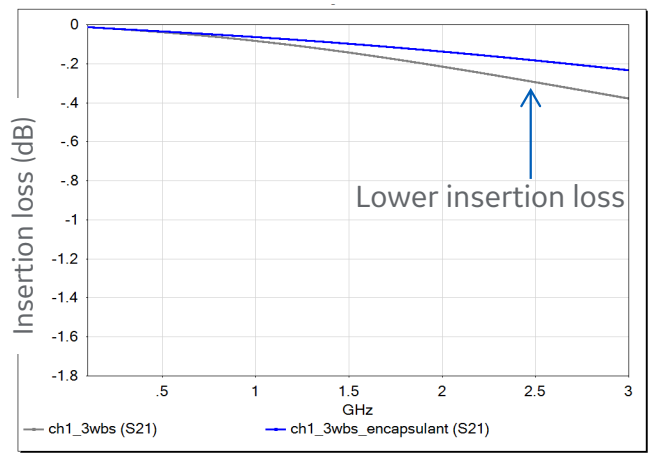
Encapsulant Effect

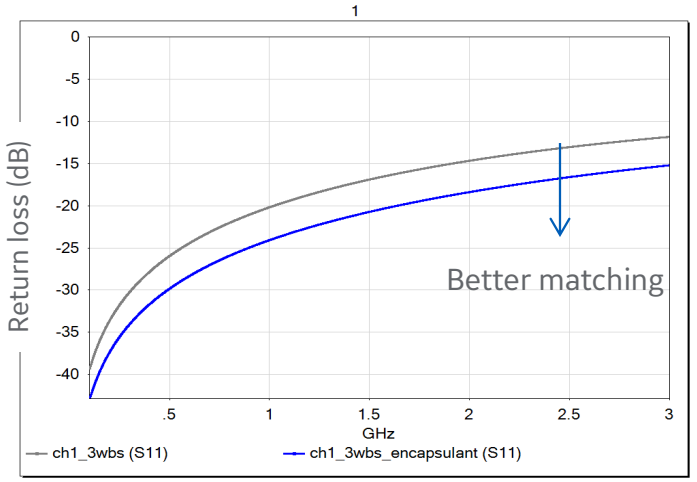
Simulation Results



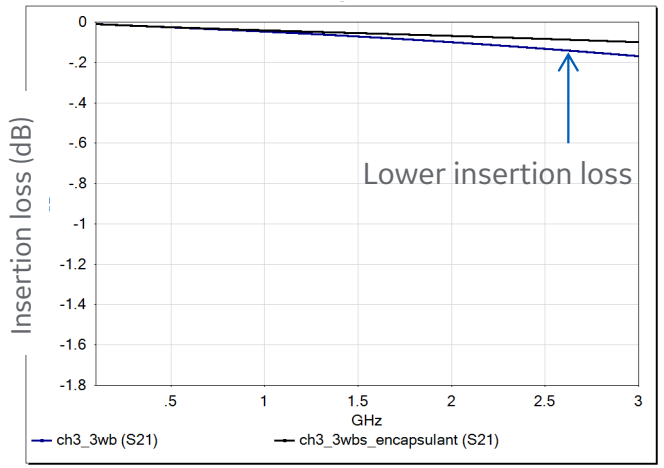
Epoxy encapsulation
- Er:3.5
- Tand:0.012

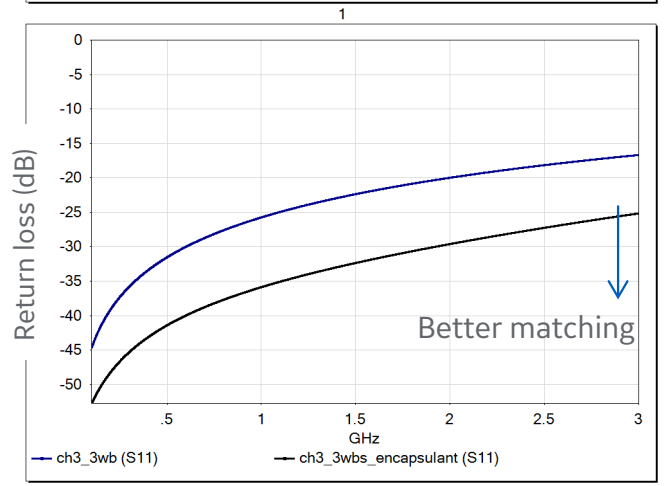
Ch. 1





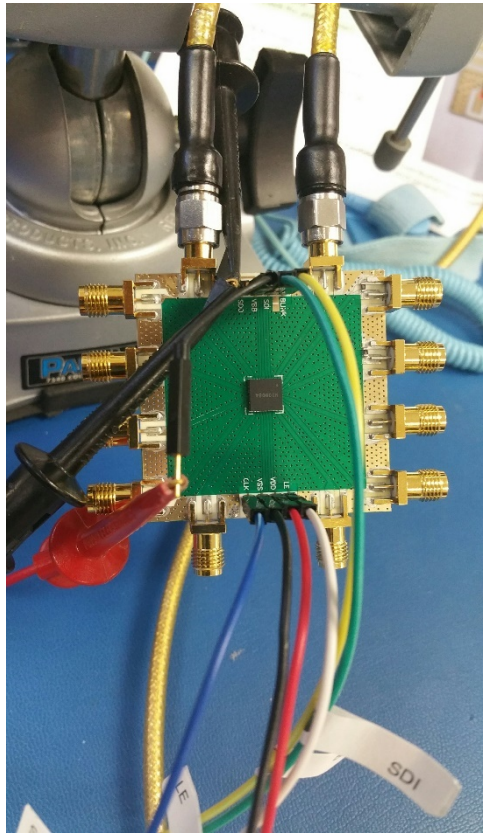
Ch. 3



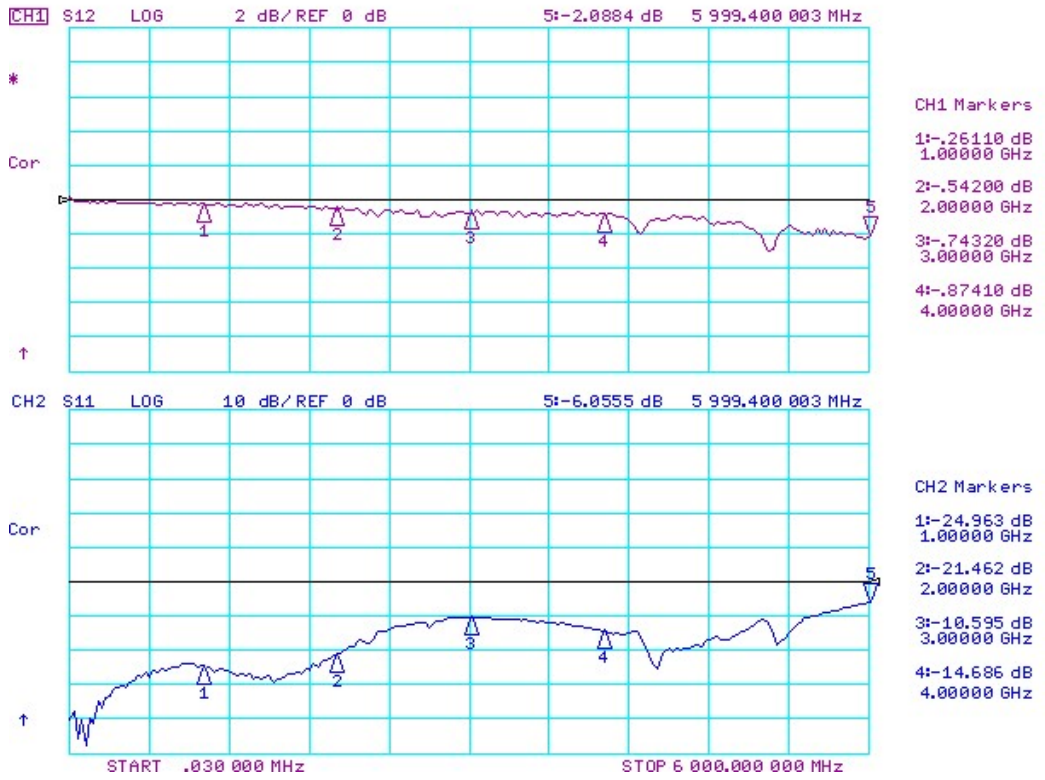


Both Ch. 1 & Ch. 3 show improvement of insertion loss and return loss due to the better impedance matching from the dielectric loading of the encapsulant material

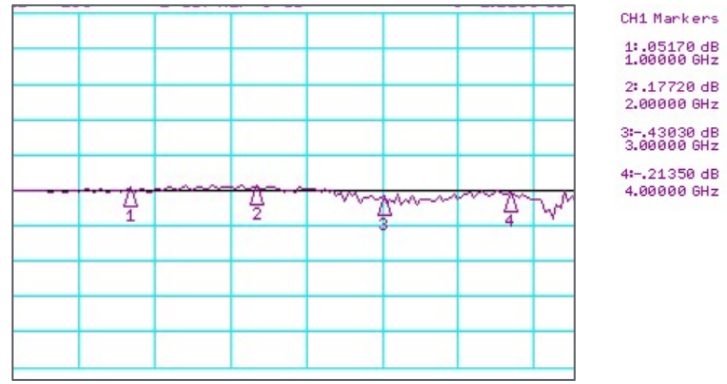
RF Electrical Testing



Evaluation kit



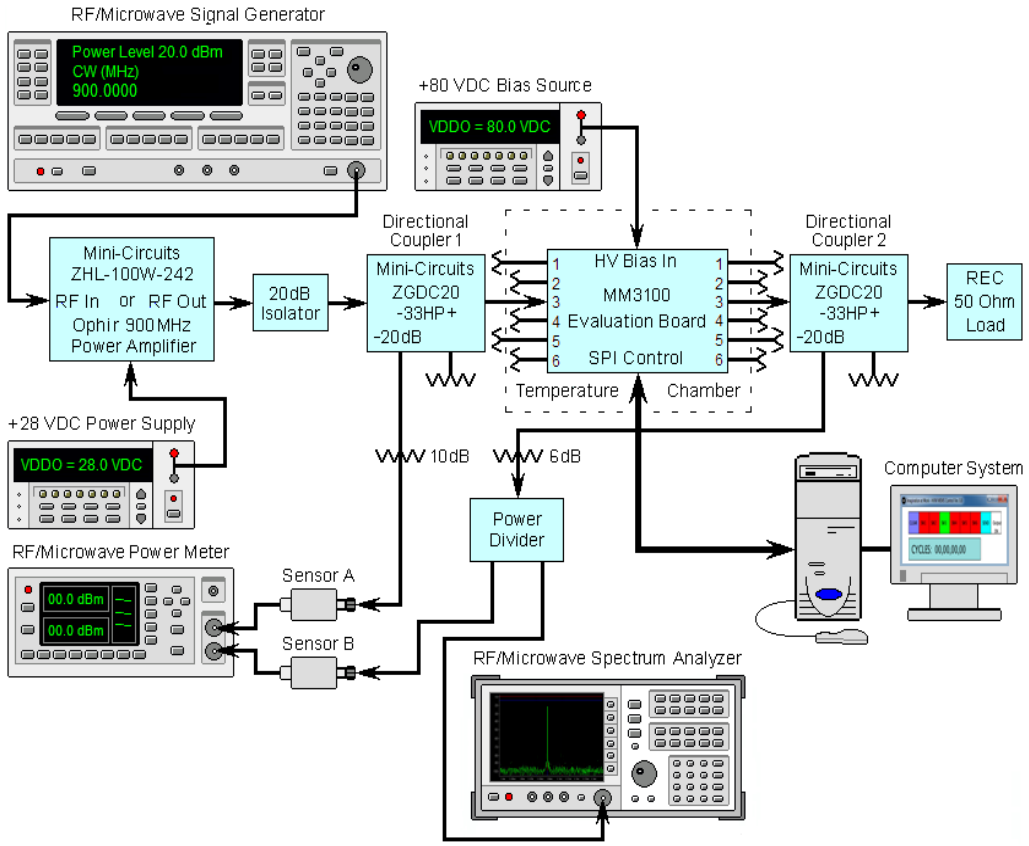
Test Results – Insertion and Return Loss



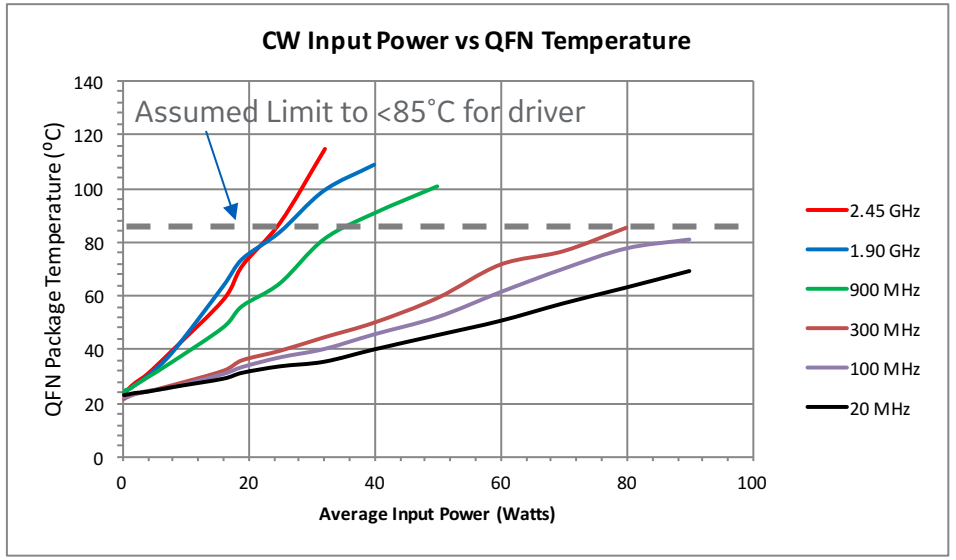
De-embedding up to package

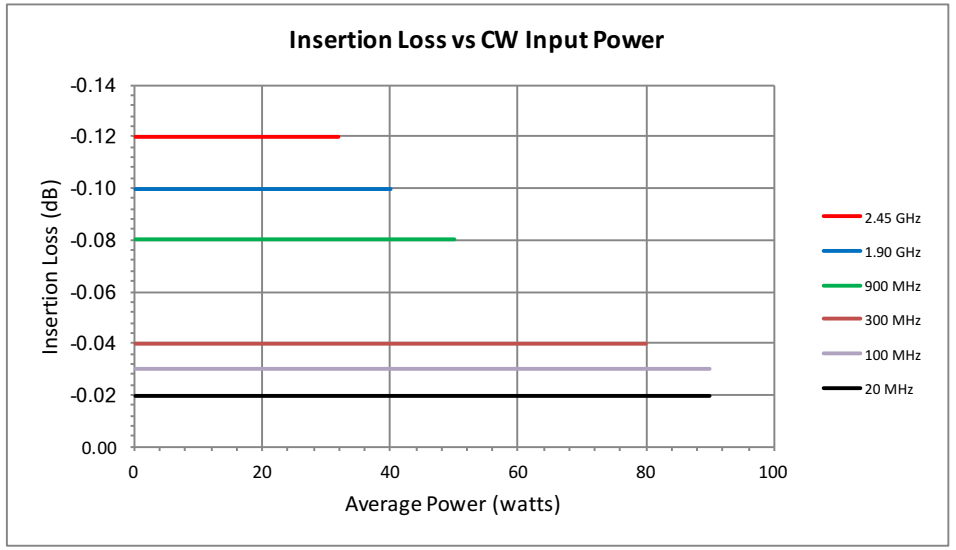
- Simulation results match experimental data
- Low On-State Insertion Loss < 0.3 dB @ 3 GHz

RF Power Testing



- Test conducted at -40C, 0C, RT, 70C, 85C
- With and without forced convection
- 25 Watt (CW), 200W (Pulsed) Max Power Handling





Test Results

Package Rel/Pre-Qual Test

Stress Test Name	Code	Condition	Status
Life test (cold)	RTOL	>10B* cycles @ RT	Pass
Temperature Humidity Bias	THB	85°C*/85%RH Held closed Biased to failure taret 500hrs JESD22 A101	Pass
85°C/85%RH storage	85-85	85°C*/85%RH 1000 hours	Pass
Pressure pot unbiased (PPOT)	PPOT	121°C* @ 15PSIg* 168 hrs	Not started
Unbiased HAST	UHAST	130°C* @ 85%RH 100 hrs	Pass
Temperature Cycle (TMCL)	TMCL	-40C* to 125C* 1000x JESD22 A104 Cond.G	Pass
High temp storage (HTS)	HTS	125°C*/1000hrs	Pass
ESD	ESD	HBM Class 0	Pass
Solder shock	WAVE	260°C*/10 sec* dip	Pass
Preconditioning	MSL	MSL 3	Pass
Drop/Shock	DROP	JESD22 B111 1,500g (0.5ms)	Pass
Vibration	VIB	JESD22 B103B Cond 1 20g*	Not started
Reworkability	REWORK	3x Pb-free SAC reflow	Pass

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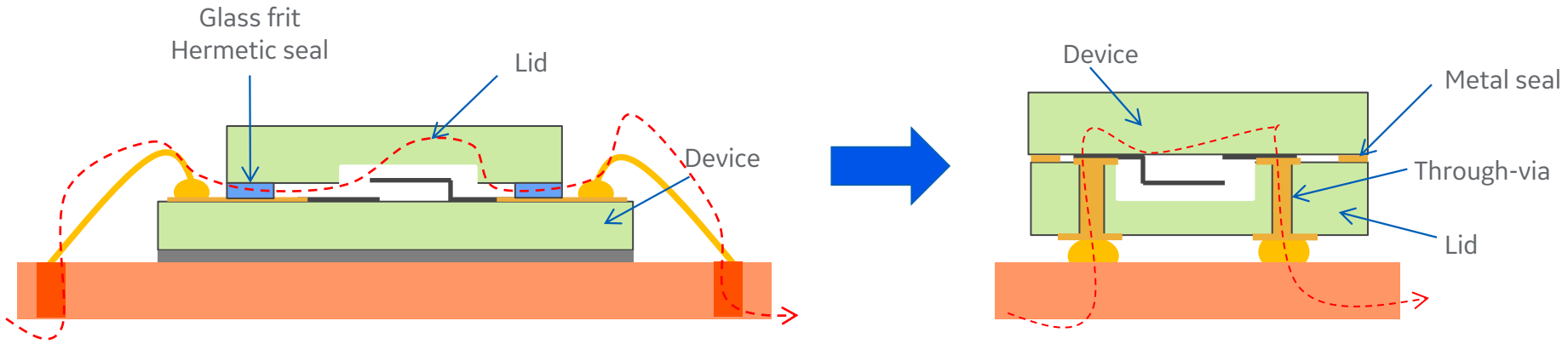
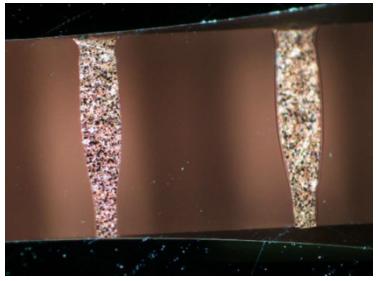
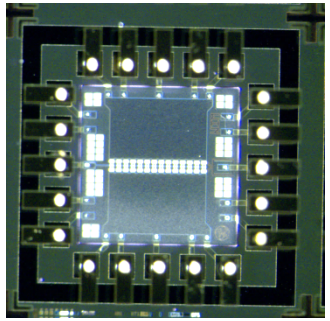
Package Miniaturization

- Flip Chip assembly

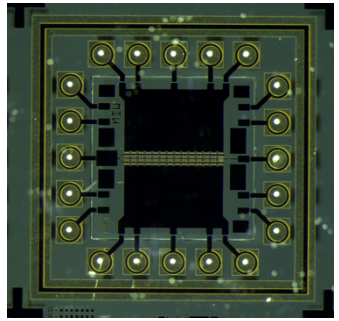


- Metal seal for hermeticity





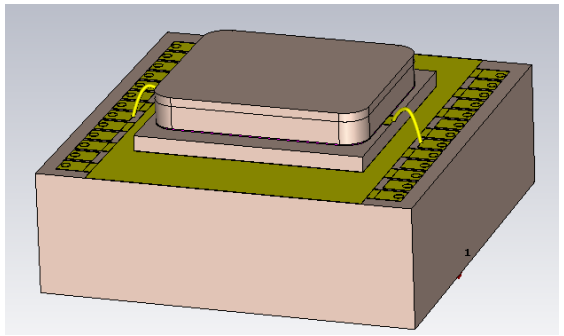
Cap view



Backside view

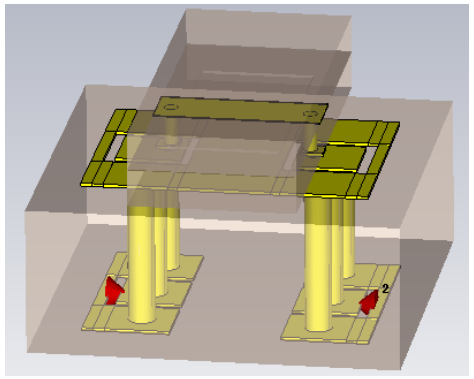
New Package Development

Today: Glass frit based hermetic package

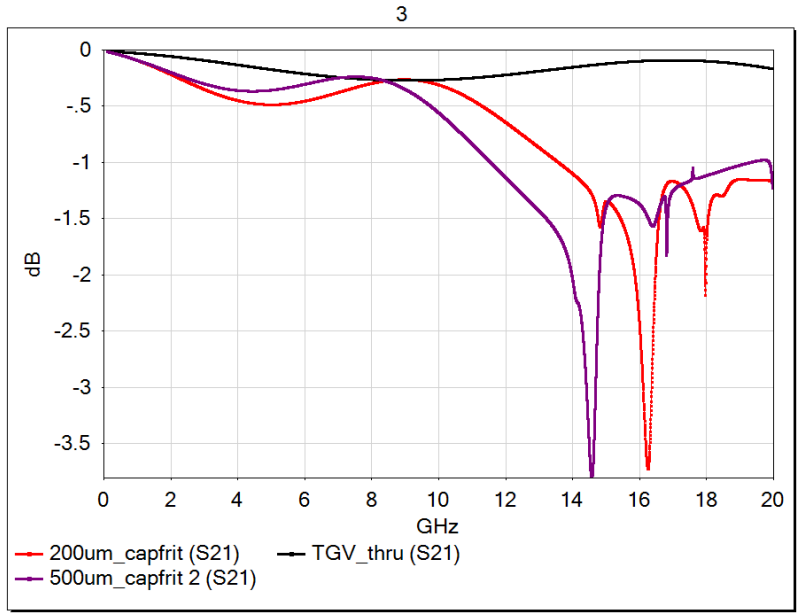


500um wide glass frit

Future: Thru Glass Via (TGV) package



Thru glass via



Glass Frit Sealed Wafer Level Package

- Large die: needs escape routing past frit line
- Low package I/O density

TGV Package

- Metal seal ring
- TGV IO's: short trace lengths
- Very high package I/O density
- Low temp WLP process

	500um frit pkg (Base line)	TGV capping
Length (L)	6mm	2mm
Package Height (H)	1.2mm	0.8mm
Insertion loss in dB @ (1, 10, 20GHz)	0.09 0.56 1.20	0.03 0.26 0.16

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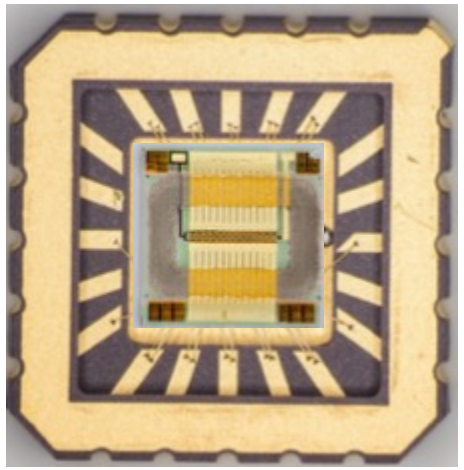
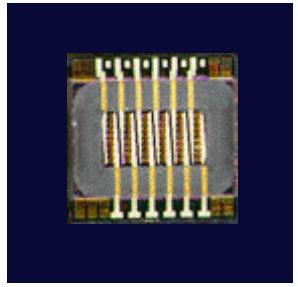
MEMS Packaging Roadmap

2014-2015
MM7100



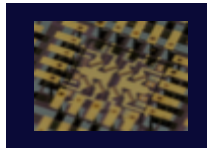
WL Glass Cap
in **9x9mm** package

2016-2017
MM3100



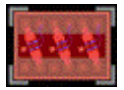
WL Glass Cap
in **6x6mm** QFN

2018



WL Glass Cap
w/TGV
4x4mm SiP

2019



WL Glass Cap
w/TGV
1x1.3mm CSP

Continuous shrink of both die and package

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Please contact us for more information:

sales@menlomicro.com

THANK YOU!